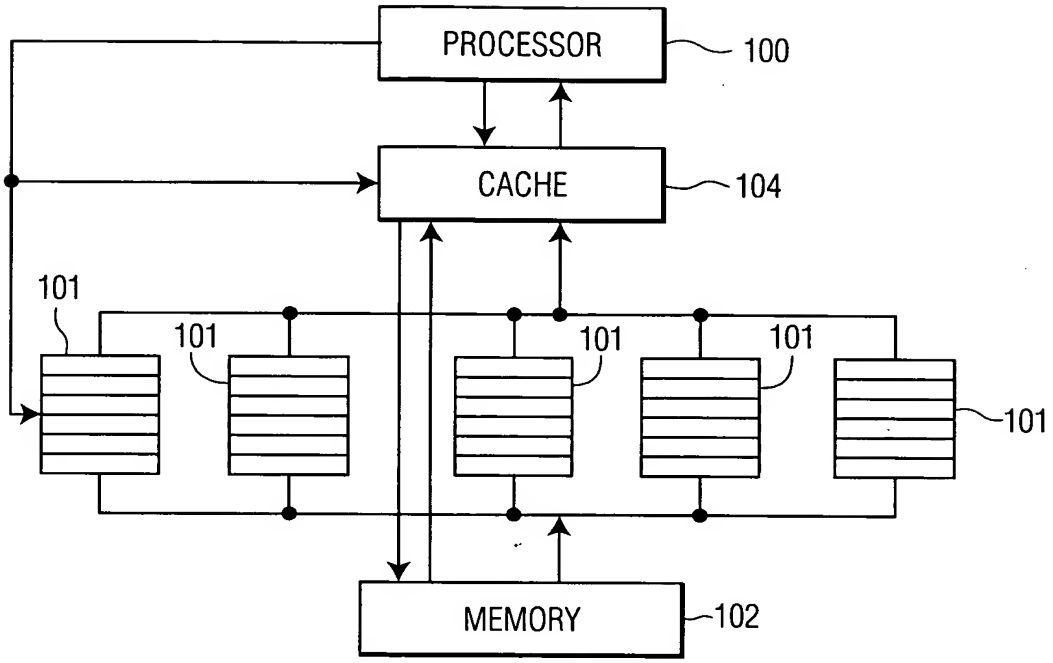


FIG. 1a
PRIOR ART

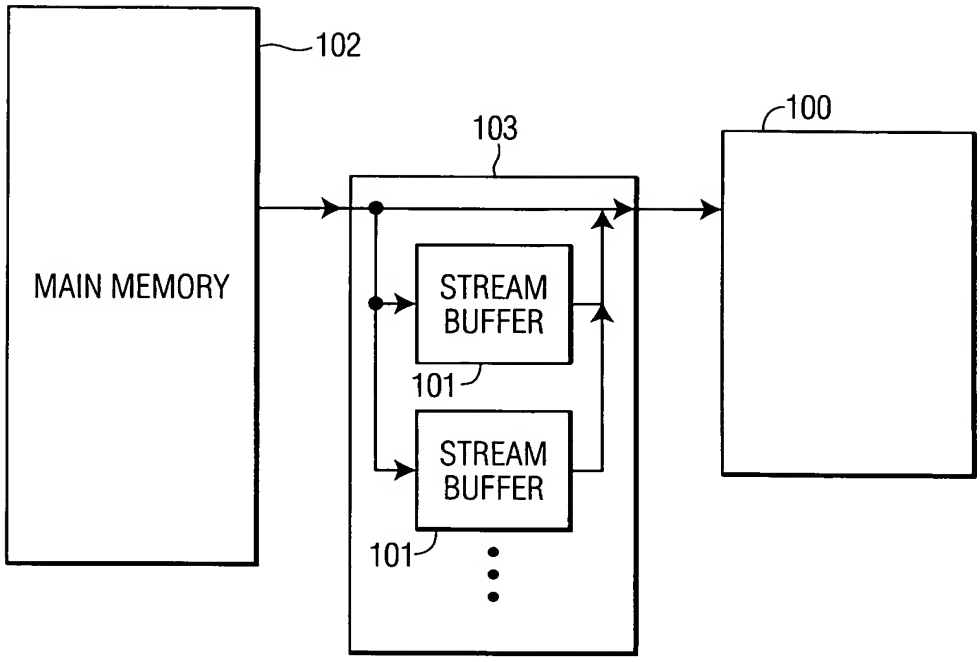


FIG. 1b
PRIOR ART

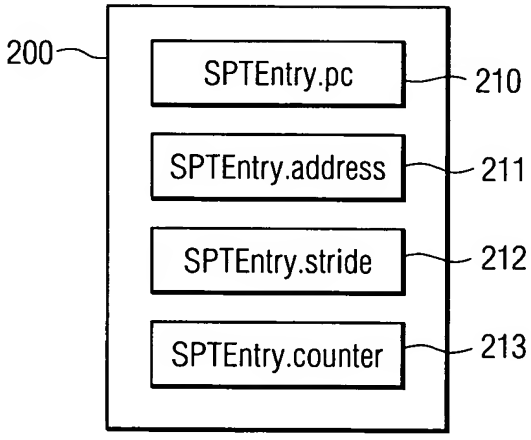


FIG. 2
PRIOR ART

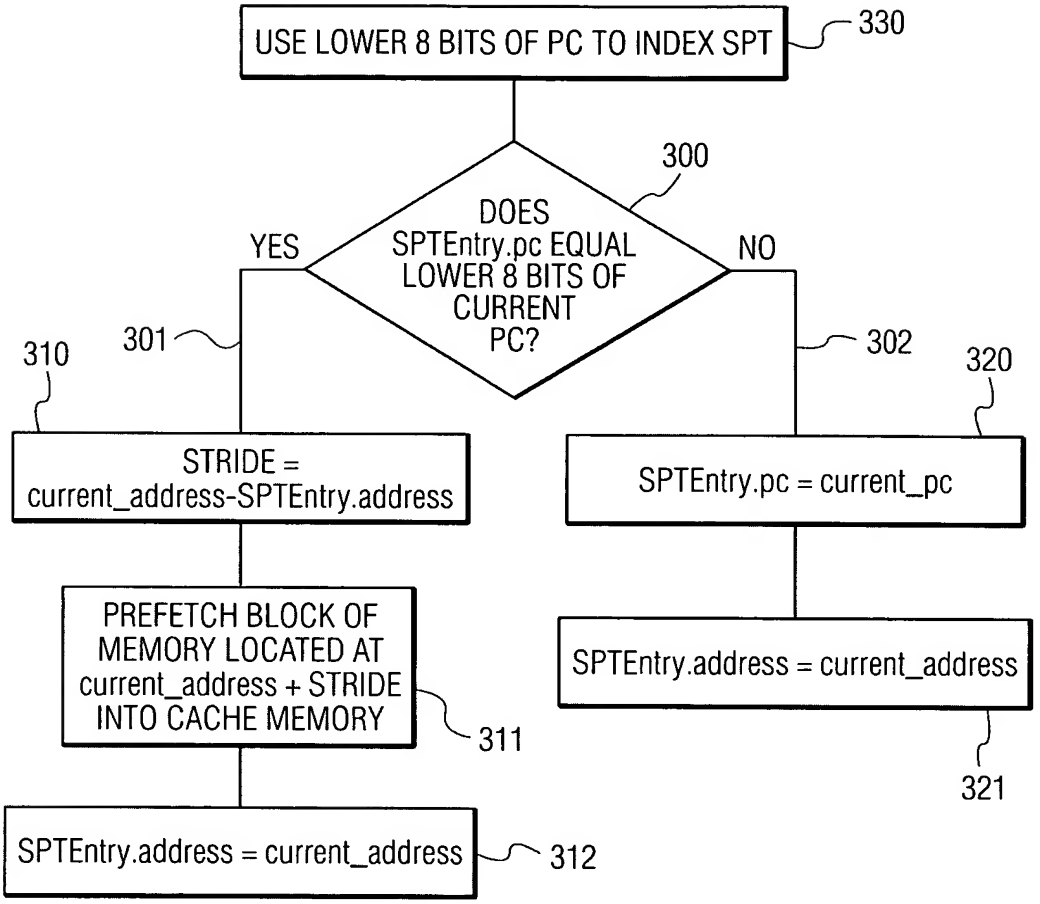


FIG. 3
PRIOR ART

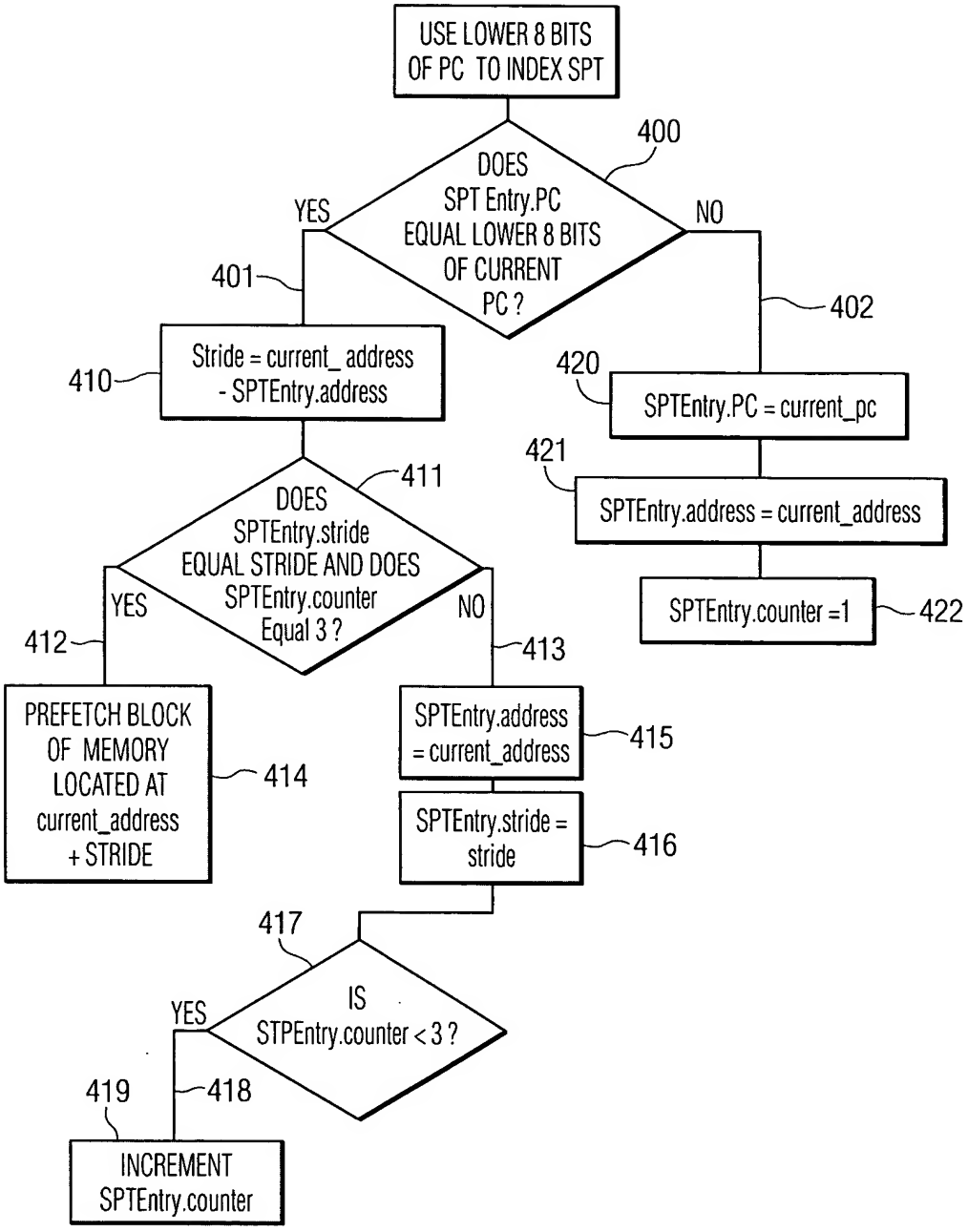


FIG. 4
PRIOR ART

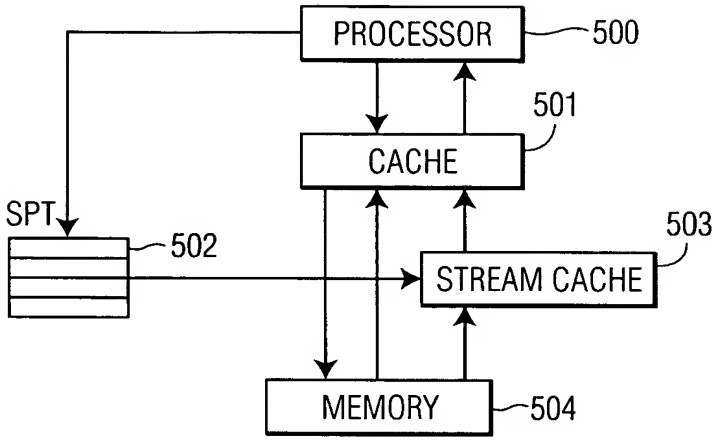


FIG. 5a
PRIOR ART

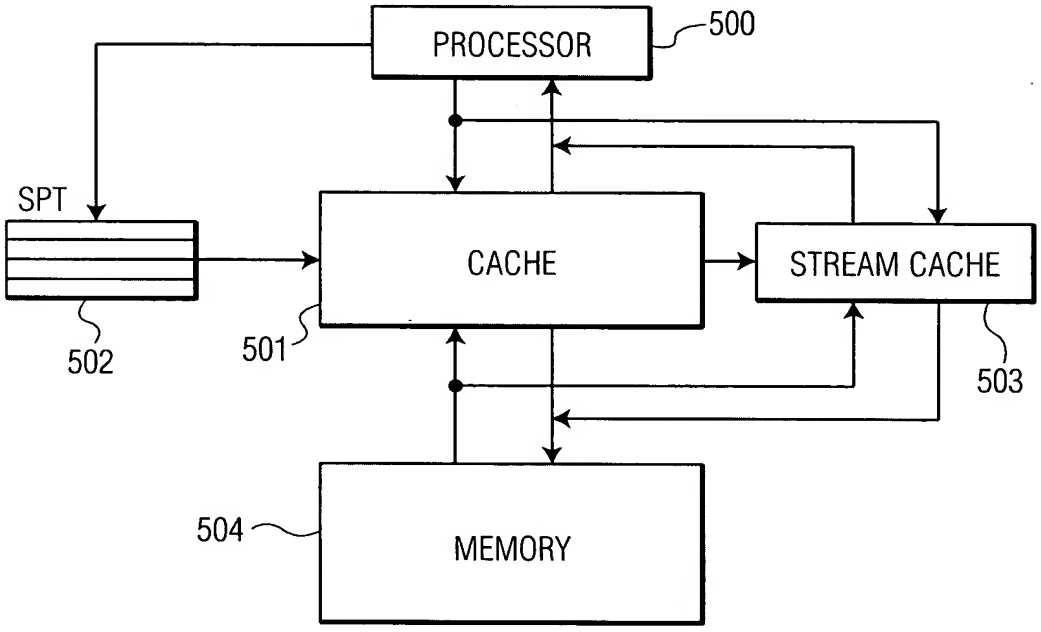


FIG. 5b
PRIOR ART

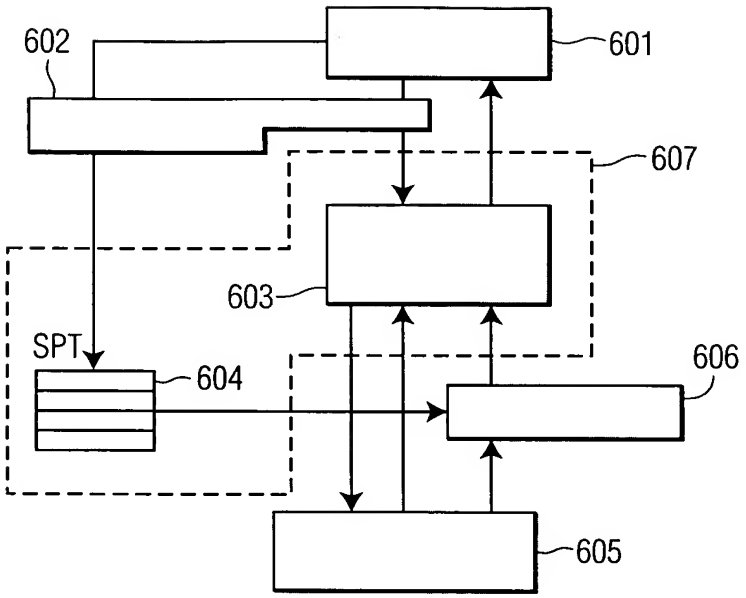
602
601
607
603
SPT
604
606
605

FIG. 6a

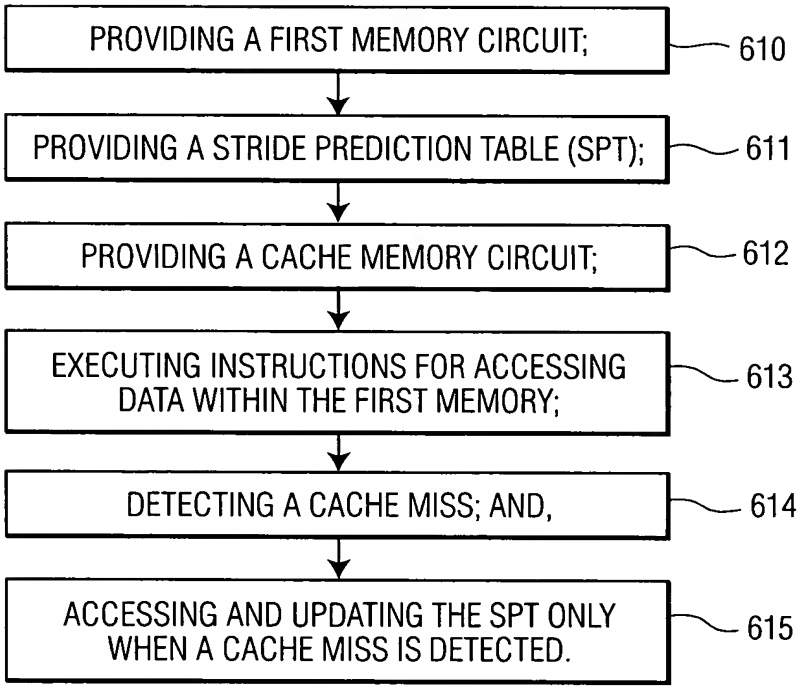
PROVIDING A FIRST MEMORY CIRCUIT;
610
PROVIDING A STRIDE PREDICTION TABLE (SPT);
611
PROVIDING A CACHE MEMORY CIRCUIT;
612
EXECUTING INSTRUCTIONS FOR ACCESSING DATA WITHIN THE FIRST MEMORY;
613
DETECTING A CACHE MISS; AND,
614
ACCESSING AND UPDATING THE SPT ONLY WHEN A CACHE MISS IS DETECTED.
615

FIG. 6b

```
I32 a[N];  ~701
I32 b[N];  ~702

for (i = 0; i < N; i += 1) {
    a[i] = b[i];
}
```

FIG. 7a

```
I32 a[N];  ~701
I32 b[N];  ~702

for (i = 0; i < N/2; i += 2) {
   a[i]   = b[i];
   a[i+1] = b[i+1];
}
```

FIG. 7b

```
I32 a[N];  ~701
I32 b[N];  ~702
I32 sum = 0;  ~703

for (i = 0; i < N; i += 1) {
   if (a[i] >= 0) {
      sum += b[i];
   }
}
```

FIG. 7c